

Real-time Video Processing  
integrating GEDAE, FPGA and VHDL

GUC 2  
PHILADELPHIA USA  
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# 1. Contents

- Video Processing Introduction

  - what is it?, why needed?, why real-time?

- Video Processing : An Overview

- Multiple Object Tracker - a real-time VP problem

- GEDAE needs & developments for VP support via FPGA firmware synthesis

- Summary

## 2. VP - Introduction

### -VP what is it?

- Processing of live video from one or more cameras to enhance image or extract information for use by operator or support system

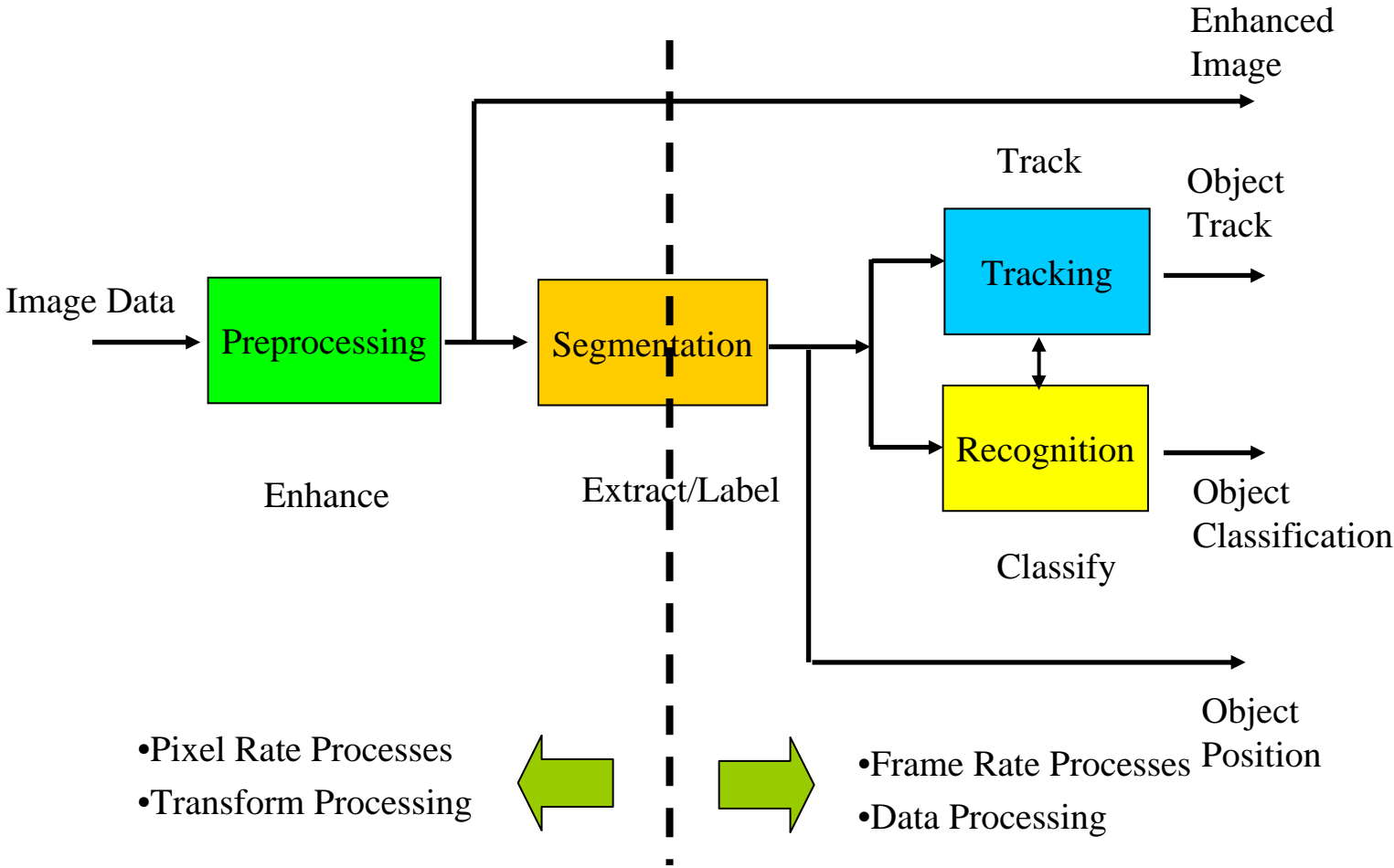
### -VP why needed?

- MIL requirements for detect, track and ATR/I
- Increasing global security threat.
  - Growing need to directly protect the public and our key facilities

### -VP why real-time? - i.e. at sensing rate, minimum latency

- In MIL and critical security/surveillance applications high rates of data availability with low latency are essential

### 3. VP - Typical Processing Block Diagram



## 4. VP - Typical VP Functions

### -Preprocessing

#### -Processes

- Noise reduction
- Edge enhancement
- Edge detection

#### -Algorithms

- FFT
- FIR
- Convolution Filter
- Temporal Filter

### -Segmentation

#### -Processes

- Feature Extraction
- Region Labeling
- Object / Area Location

#### -Algorithms

- Clustering
- Region Growing
- Boundary Extraction
- Shape Measurement
- Correlation
- Centroid

### -Track / Recognition

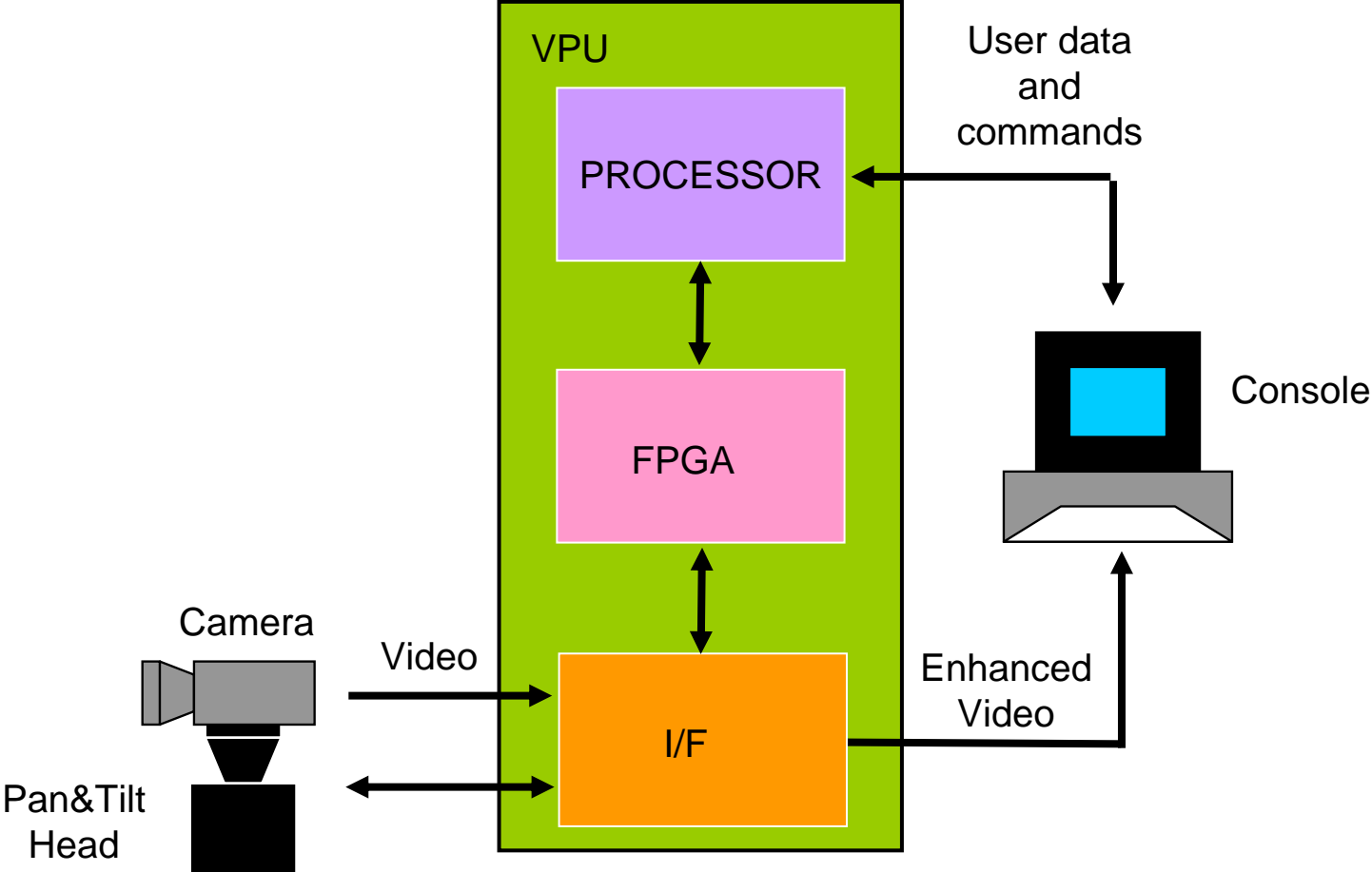
#### -Processes

- Object Track
- Classify

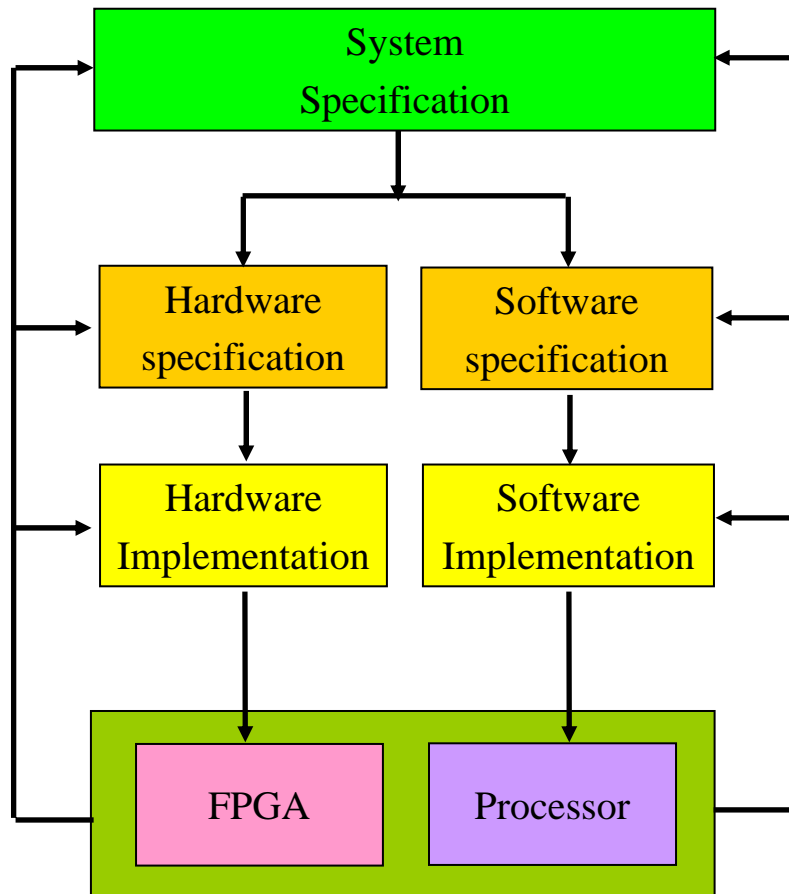
#### -Algorithms

- Simple Linear
- Kalman Filter
- ANN
- Bayesian
- Geometric

# 5. Video Processor Architecture

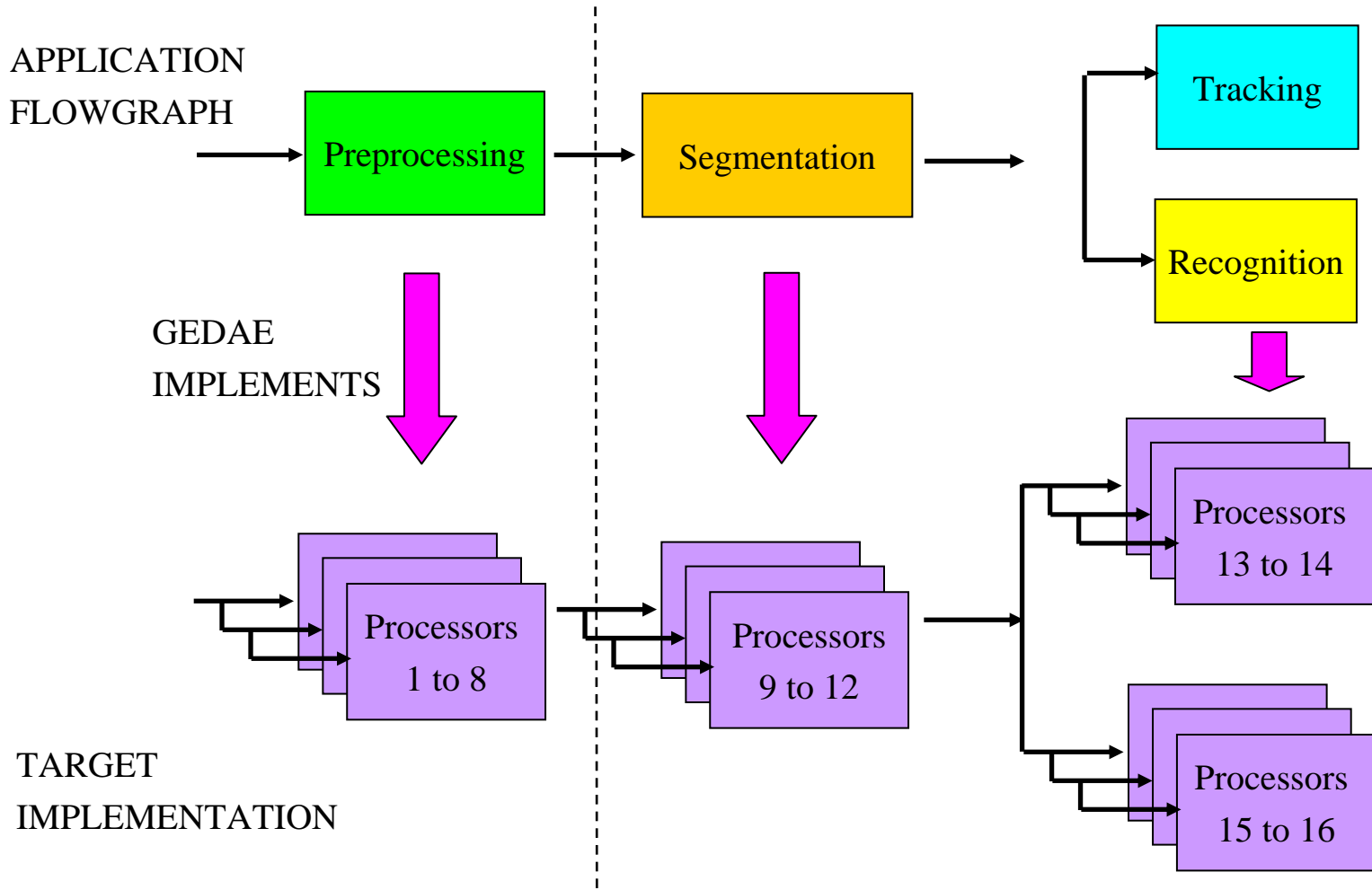


## 6. Conventional Implementation Approach

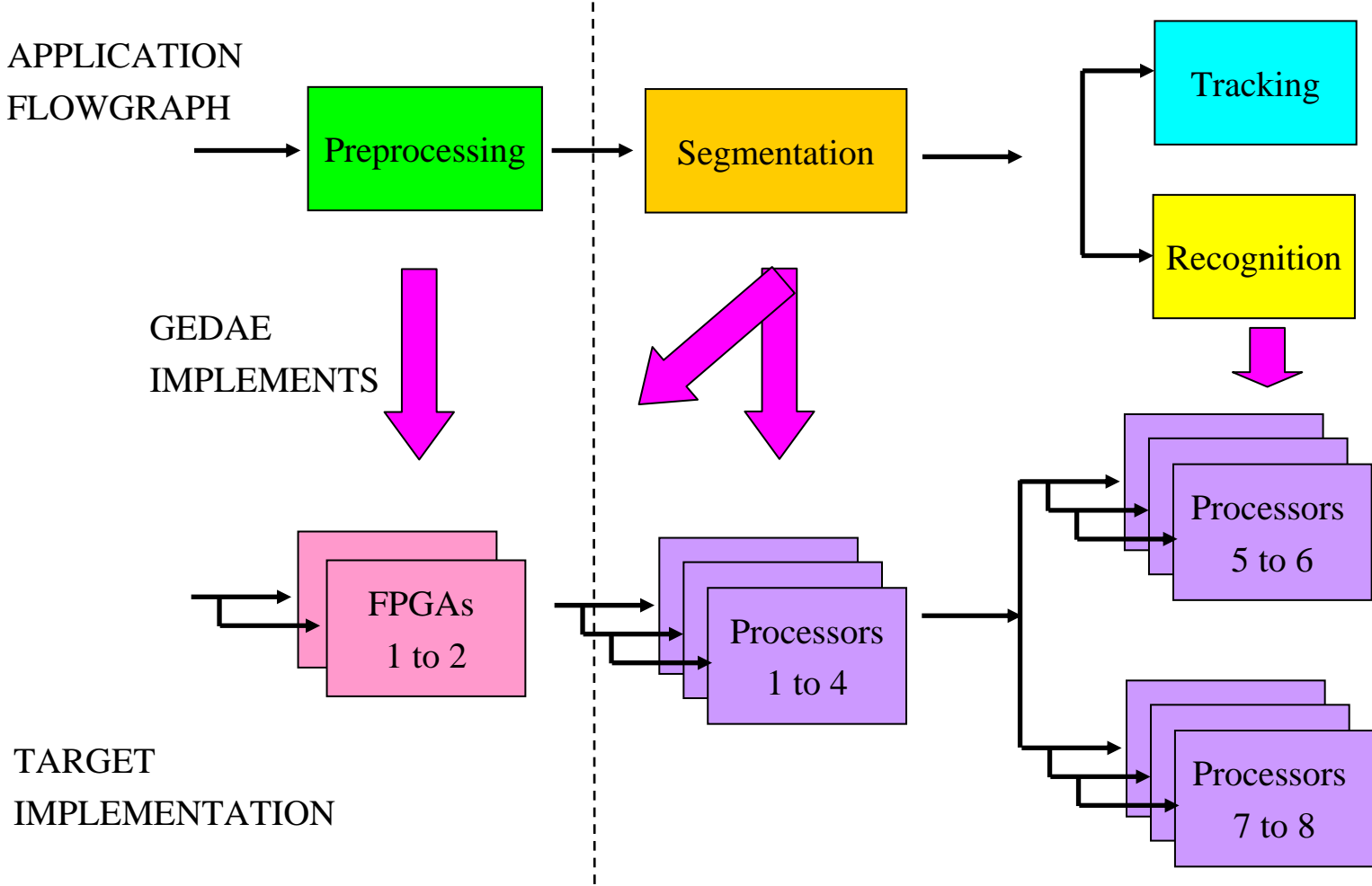


- SYSTEM SPECIFICATION
  - MATLAB/SIMULINK, MATHCAD, C/C++
  - ...
- HARDWARE : FIRMWARE
  - MENTOR ...
  - XILINX, ALTERA ...
  - VHDL
  - VERILOG
- SOFTWARE
  - GEDAE
  - RHAPSODY
  - C/C++, ADA ...

# 7. GEDAE - Conventional "MP2" Software Mapping



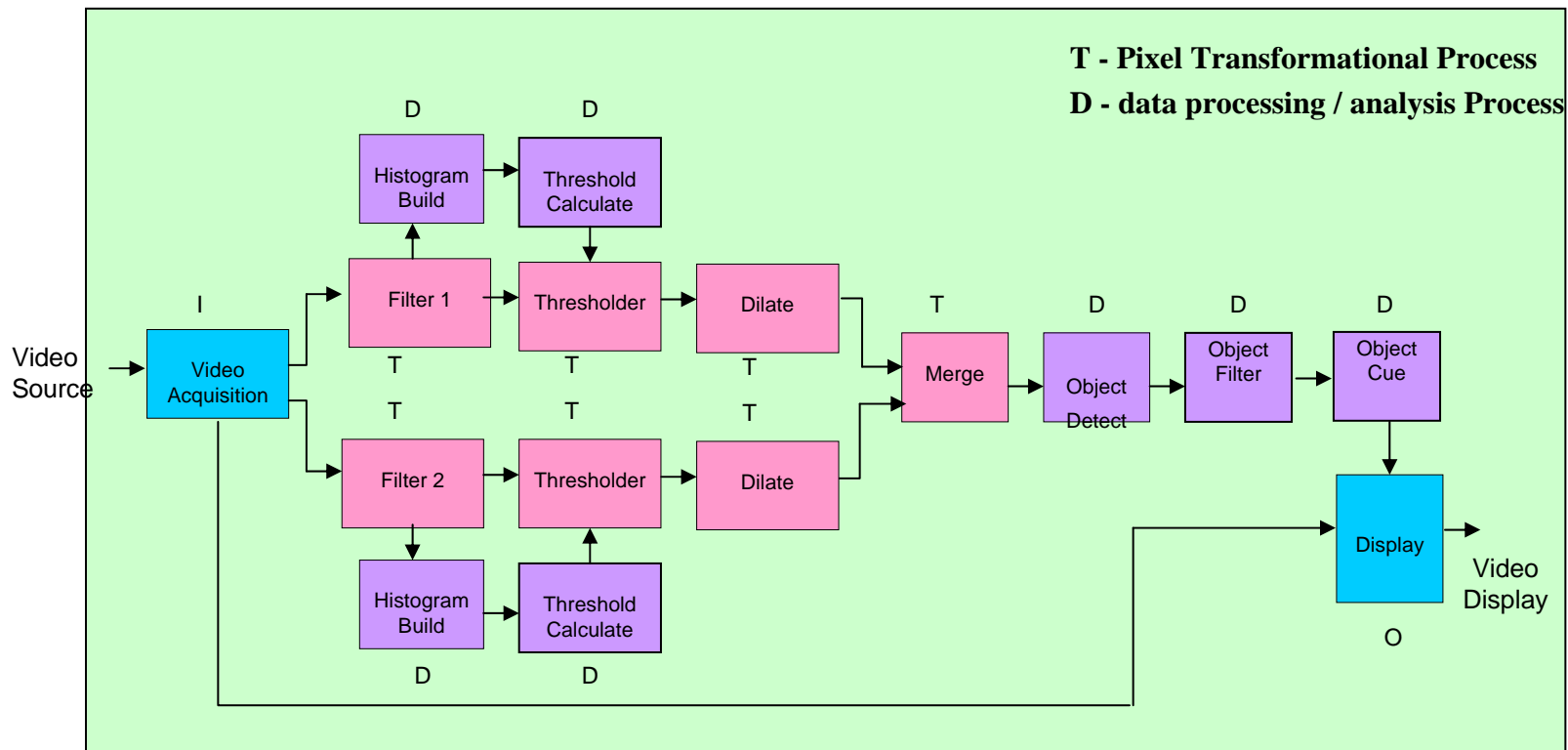
# 8. GEDAE - Potential Approach : Firmware/Software Mapping



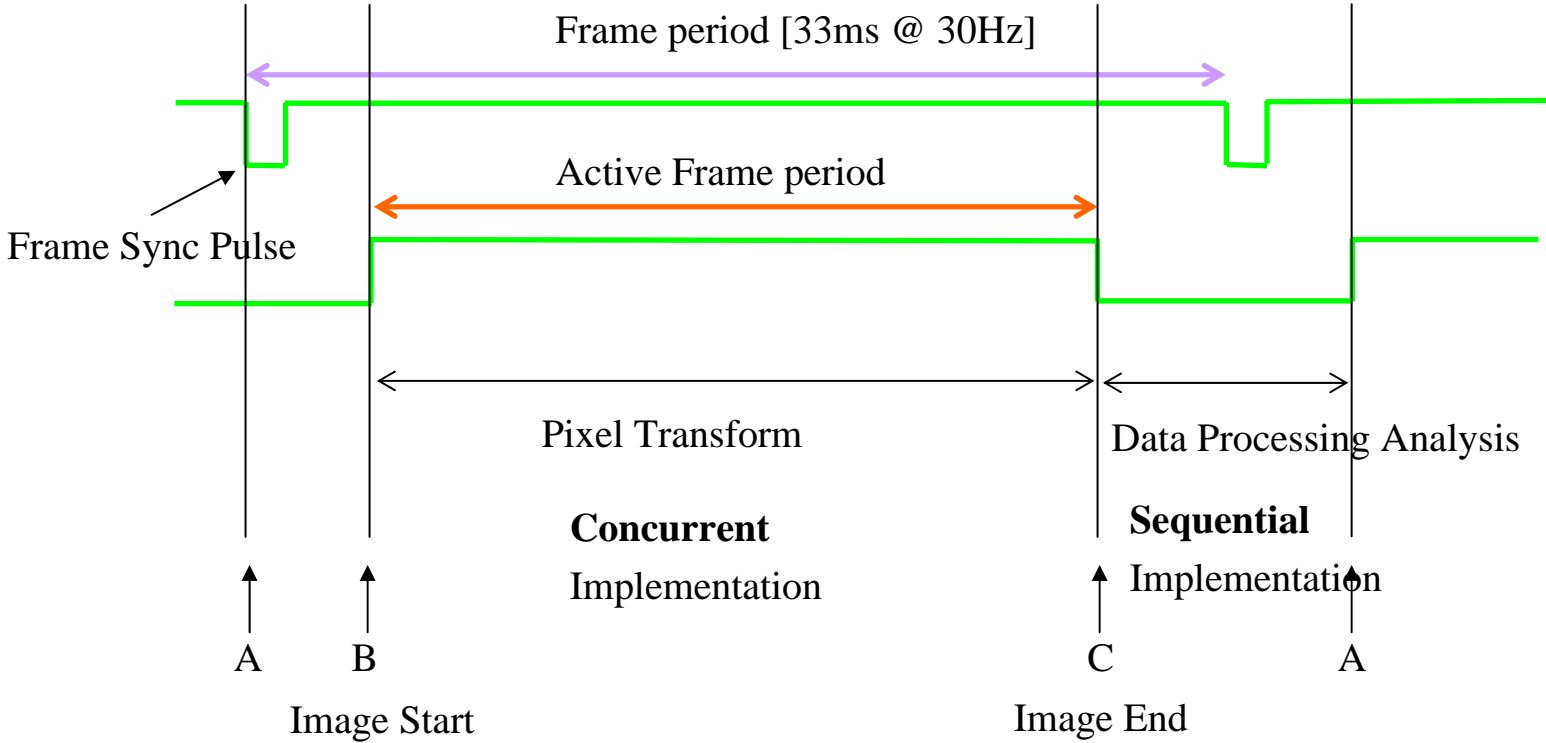
## 9. MOT Specification

- Detect and track up to 16 objects in input video
- Highlight tracked objects on output video
- input video : 30 fps, 640 x 480 pixels/frame
- output video : 60 fps, 640 x 480 pixels/frame
- Throughput : 30 frames/sec, no dropped frames
- Latency < 1 frame period

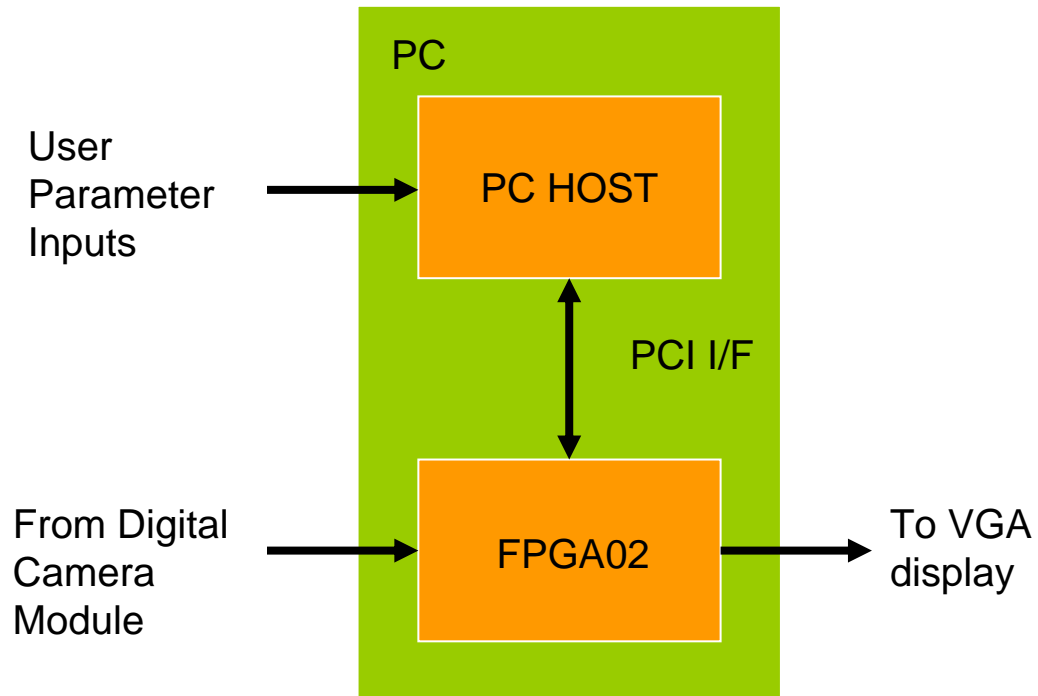
# 10. MOT Block Diagram



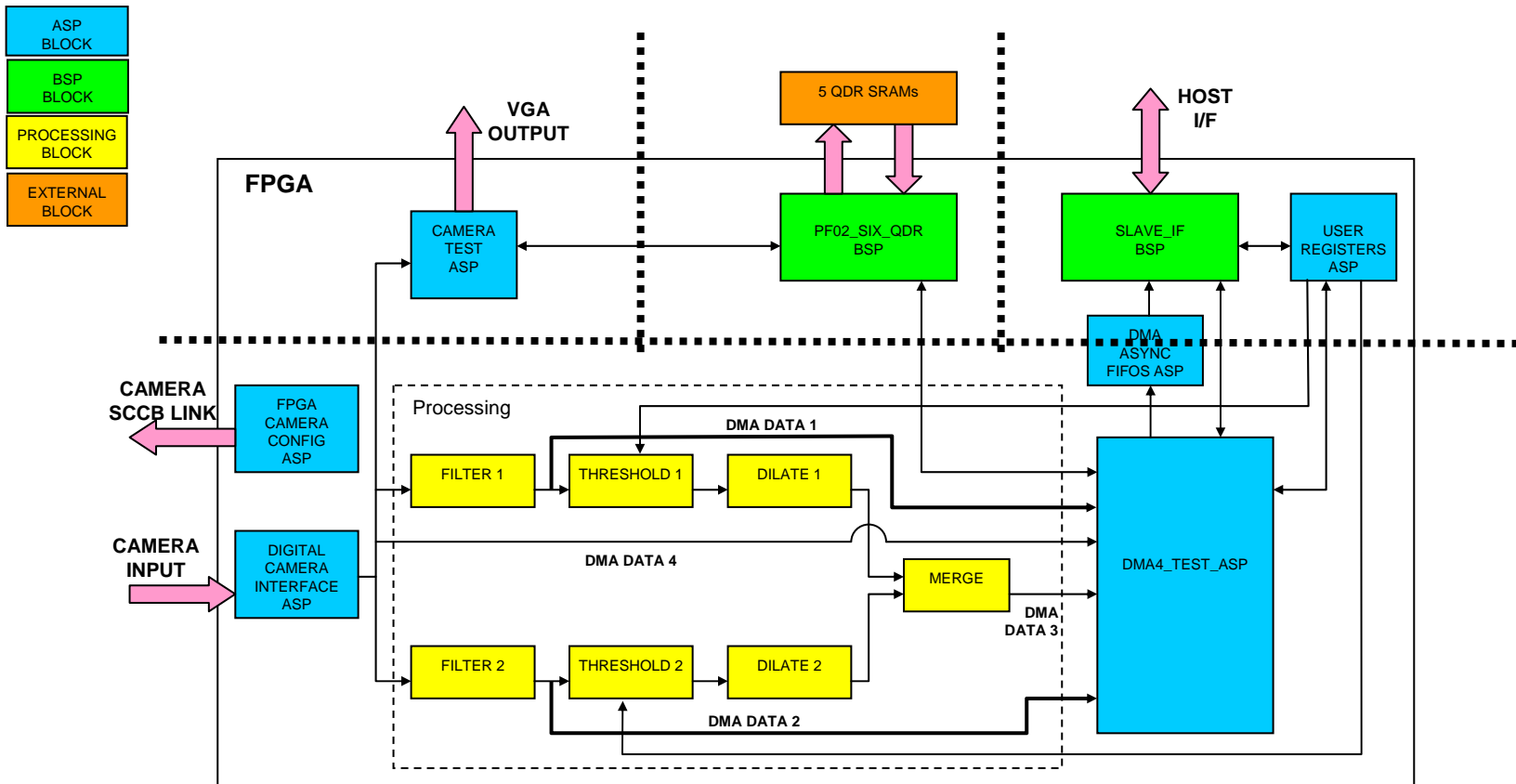
# 11. MOT Performance : Implementation Timing & Control



## 12. FPGA02 Demo Configuration

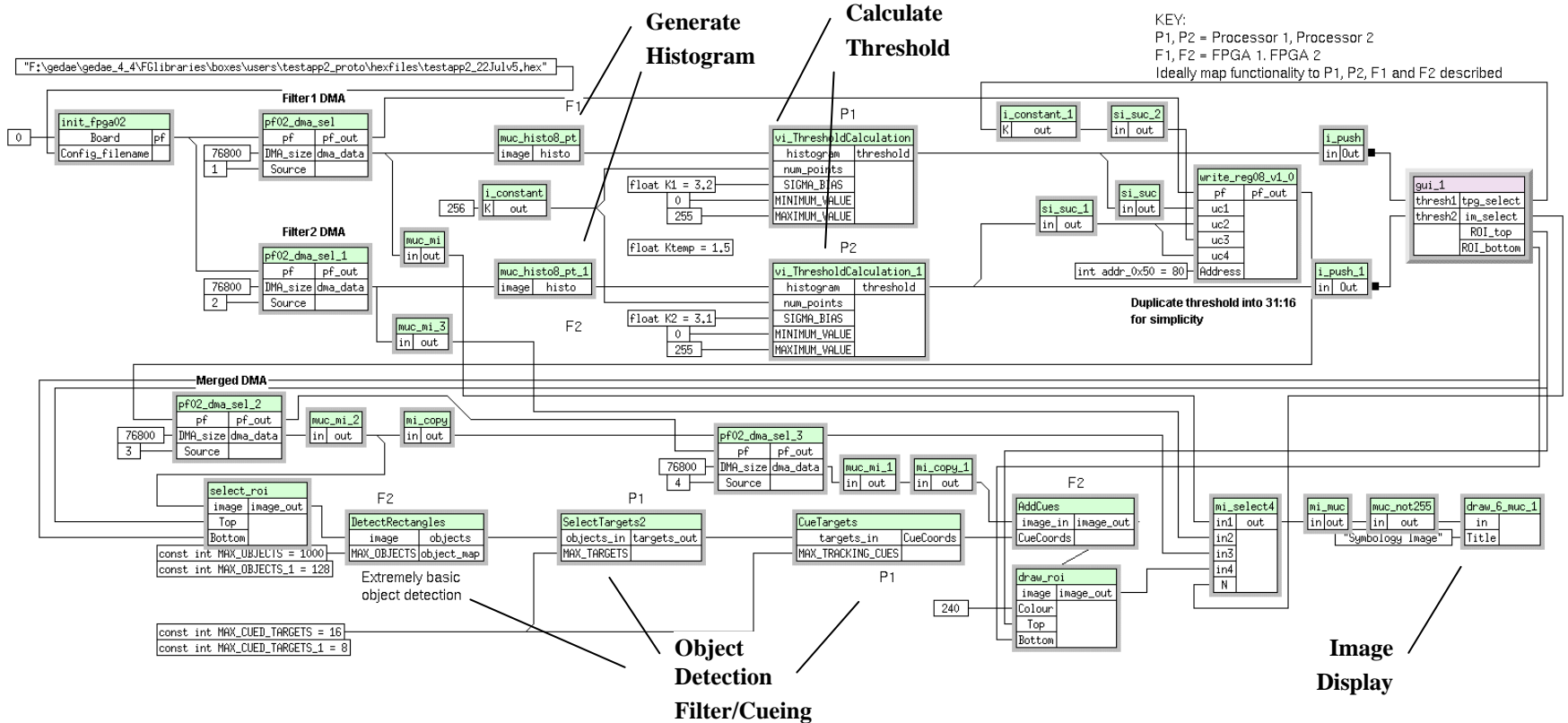


### 13. MOT Implementation(1) - FPGA02 Firmware Diagram



..... Clock domain boundaries

# 14. MOT Implementation(2) - Software GEDAE Flowgraph



## 15. Filter1 Image Example



## 16. GEDAE Support Requirements for Firmware Synthesis

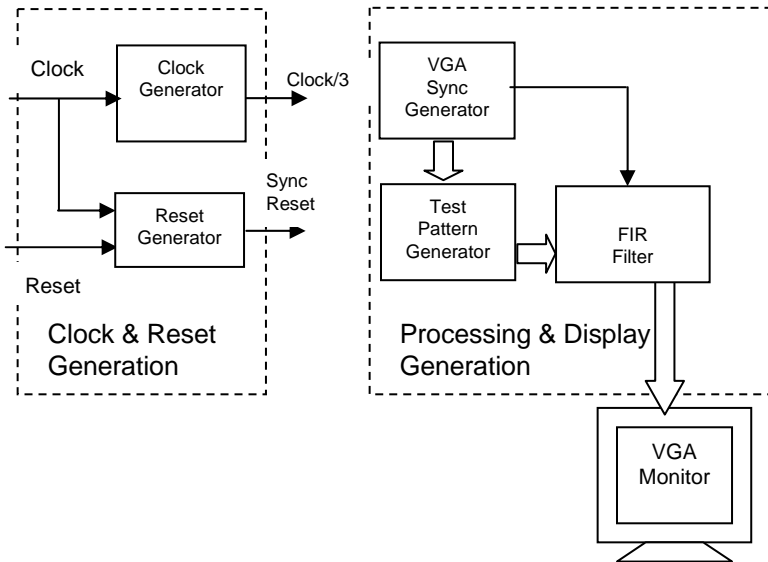
- single cycle, synchronous, clocked design entry
- multiple clock domains
- core and BSP use
- efficient vhdl code generation
- hardware trace for optimisation
- fixed point, BIT true models

## 17. GEDAE Support Developments for Firmware Synthesis

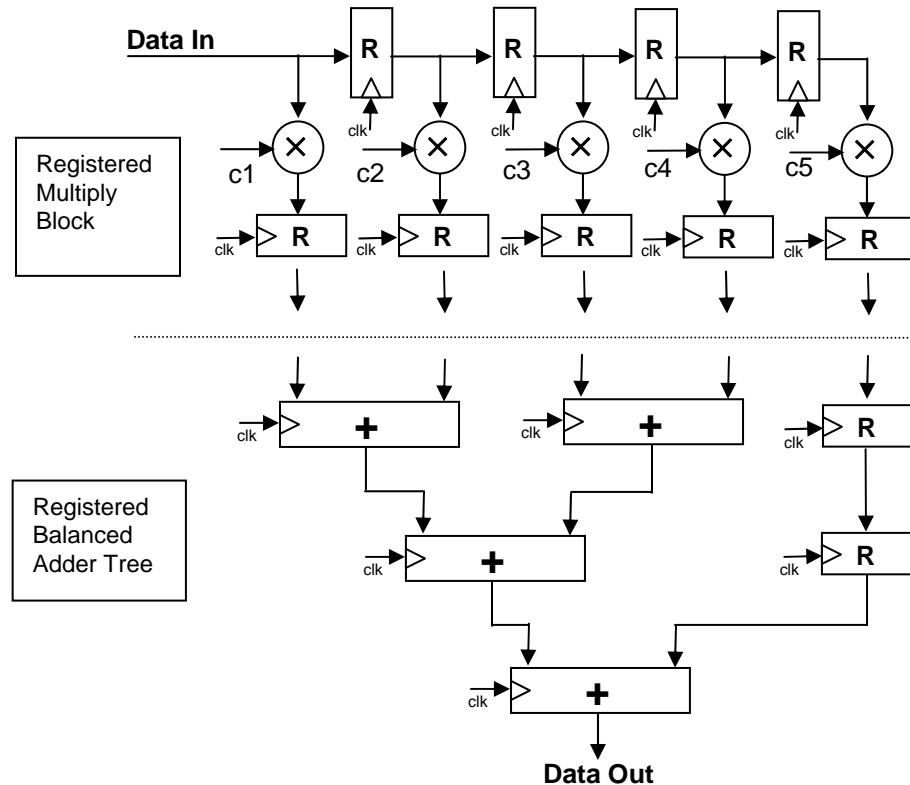
- GEDAE RTL : Single sample language
- core support
- LSP for vhdl code generation
- build process - GEDAE RTL to FPGA code
- Integration with GEDAE Environment
- FIR filter design examples

# 18. FIR Filter Reference Design

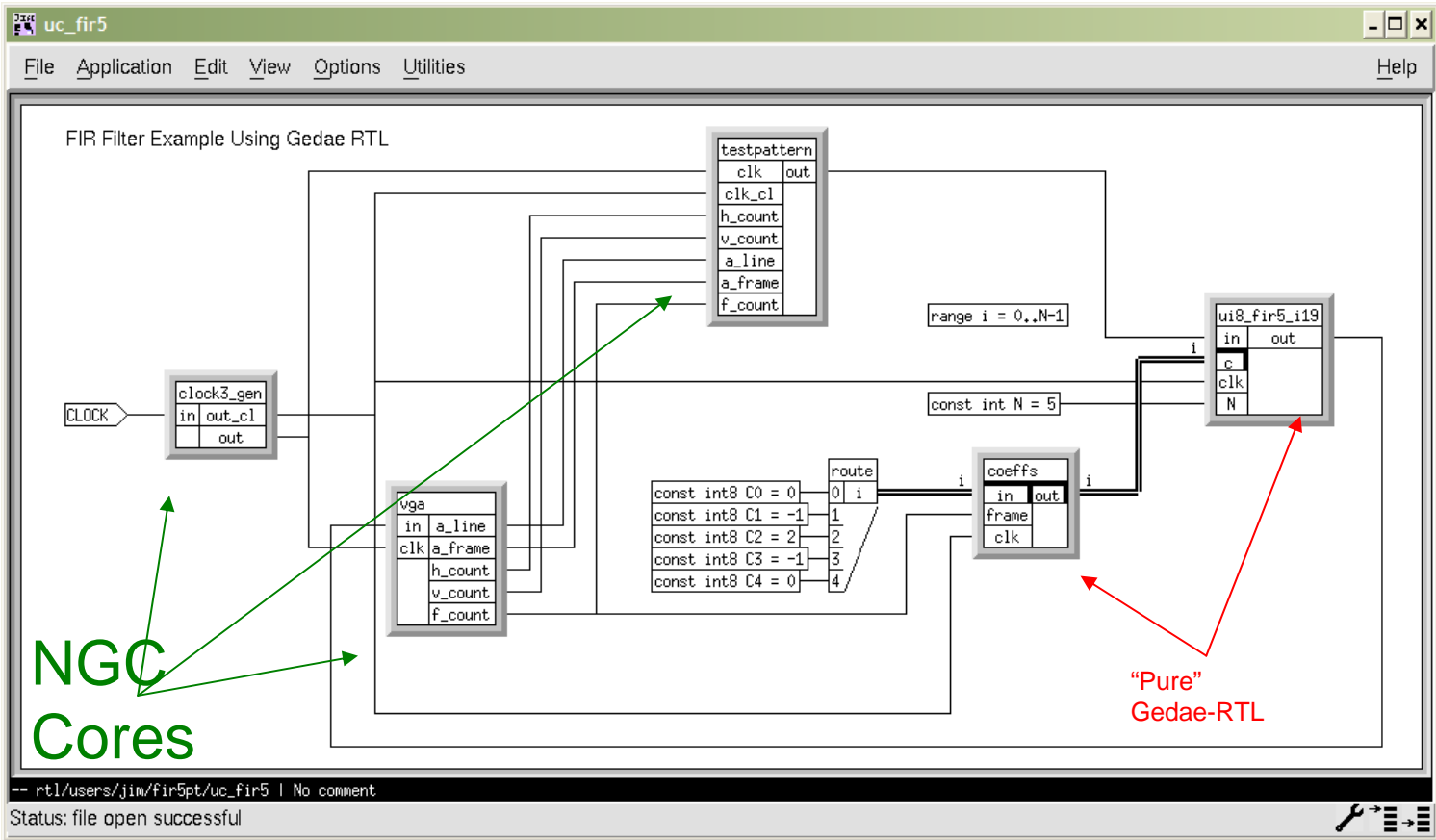
FIR Filter Ref Design Block Diagram



5 Point FIR Filter



# 19. GEDAE RTL - FIR Flowgraph



## 20. Summary

- VP applications employ a mix of FPGA and processor technologies to deliver real-time surveillance solutions
- VP is potentially a large market for tool with integrated capability for joint software and firmware synthesis
- Real-time MOT design integrating GEDAE, FPGA and VHDL technologies highlights many of the technical challenges for firmware support.
- GEDAE Initial support for FPGA Firmware synthesis within existing environment developed
- Real time VP FIR Filter examples integrating software and firmware components developed using new GEDAE heterogeneous target support