

# GEDAE and the CAPTOR Programme

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## ABSTRACT

The CAPTOR project is a multi-national European project to develop the nose radar for the Eurofighter Typhoon aircraft.

The processing solution of the CAPTOR radar needs to be re-developed, as a result of hardware obsolescence in the original radar system design. This involves re-development of the signal processing software because the existing software is designed and heavily tailored to work on the existing ASIC based processor hardware. The CAPTOR T2 Signal Processing Software will be developed jointly by BAE SYSTEMS and EADS, by the formation of a joint Systems and Software IPT, made up of engineers from both companies and based at sites in Edinburgh (UK) and Ulm (Germany).

The GEDAE tool from Blue Horizon Development Software (BHDS) was identified as the primary candidate tool to support the redevelopment of this software, mainly due to its applicability to the type of algorithms being implemented and its ability to port to targets and optimise processor loading.

A licensing arrangement agreed between BHDS and the CAPTOR programme was put in place which allows full use of GEDAE on CAPTOR and includes provision for significant consultancy as well as training. This relationship has allowed CAPTOR requirements to influence GEDAE development over the past 2 years to the mutual benefit of all parties.

A development process has been designed to exploit the features of the selected tools and allow the multi-site development to proceed. A pilot study has confirmed that the GEDAE tool has the capability to generate signal processing software which runs at the required speed on a representative target hardware platform. It also confirmed that the proposed development process was workable and allowed this process to be further refined.

Full scale development of the Tranche 2 Signal Processing Software is now underway. A large amount of the algorithmic functionality of the signal processing has been implemented in GEDAE and tested. The initial batch of radar modes have been developed from these algorithms and tested to verify functionality. The control structures have been developed to allow multiple modes to run in a distributed architecture. Legacy code where appropriate has been encapsulated in GEDAE wrappers and tested.

Initial benchmarking of the radar modes on representative target hardware has been carried out, and the indications are that the approach being used is generating a Host model which will run fast enough on the target with minimal modifications.

## 1. INTRODUCTION

The CAPTOR project is a joint European project to develop the nose radar for the Eurofighter Typhoon aircraft.

### 1.1 The CAPTOR Programme

The project is split into a number of phases known as Tranches. The Tranche 1 (T1) development phase is complete and the radar is now in production and following extensive flight testing on the development Eurofighter aircraft.

Preparation for Tranche 2 (T2) is now underway and unfortunately, as a result of the rapid rate of development of commercial processing systems, many of the original electronic

components used in T1 are no longer obtainable. This situation, referred to as Component Obsolescence, is not entirely negative because it does bring an opportunity to update the design and the opportunity is also being taken to put in place an infrastructure, both in terms of hardware architecture, and supporting development toolsets, that can be evolved and reused for an extended period of time.

The radar processor redevelopment is being undertaken jointly by BAE SYSTEMS in the UK and EADS in Germany.

## 1.2 Overview of the CAPTOR Radar

The main components which make up the CAPTOR radar system are shown in Figure 1.

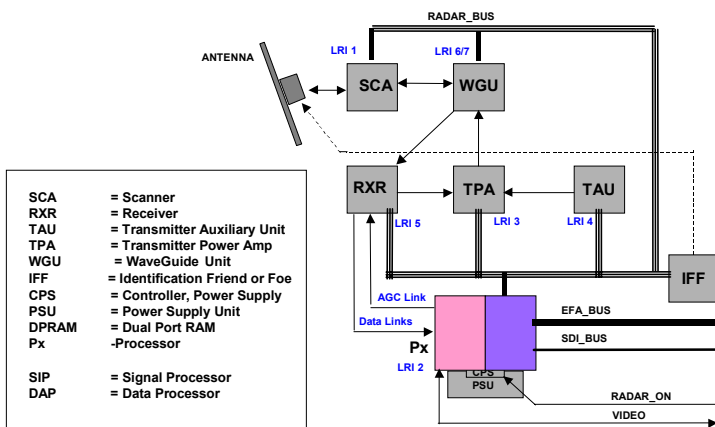


Figure 1 – The CAPTOR Radar System

The CAPTOR radar is basically made up of a Transmitter, Scanner and Antenna, Receiver and Processor. The Processor controls the operation of the radar and provides an interface to the operator. A variety of waveforms can be generated and transmitted via the antenna. The received signals are processed by the Processor, and the resulting target detections are displayed to the pilot and are also analysed by the Processor to identify target tracks. Thus the Processor is required to perform both Signal Processing (SIP) and Data Processing (DAP) tasks.

The Signal Processing task is to process digitised radar returns from the Receiver to extract targets, or in mapping modes, to create a ground map.

The Data Processing task entails target tracking, overall radar control, changing modes of operation and pointing the scanner.

## 1.3 A New Processor for Tranche 2

The Tranche 1 Processor was designed using Application Specific Integrated Circuits (ASICs) to implement a highly task optimised architecture. For Tranche 2 it is no longer necessary to use application specific components because commercial off the shelf (COTS) processing components can now achieve the necessary processing throughput. A COTS microprocessor based architecture has therefore been selected, and this is being coupled with the introduction of new, streamlined software development

processes which allow the use of modern auto-coding software development tools.

The T2radar Processor has the same overall functional requirements as at T1, and fortunately the Data Processing software, containing the essence of the radar design, can be re-hosted and reused for T2. However, the original T1 software for the Signal Processor is written specifically to run on the T1 ASIC processor hardware, and is not well suited to direct reuse on a generic microprocessor platform, so it needs to be significantly redeveloped for T2.

## 1.4 The new Hardware Platform

The CAPTOR T2 Integrated Processor (CIP) consists of multiple identical common processing modules, known as Universal Vector Processor Modules (UVPs), each housing a cluster of four G4 AltiVec PowerPC processors and associated memory and interface components all based on commercial chip sets. These are linked to the existing radar system by a single module housing custom designed FPGA chips which emulate the T1 radar processor external interfaces.

## 1.5 Finding the right tool

A number of software tools were evaluated in the late 1990's to establish which tool could provide the best development environment for the CAPTOR T2 Signal Processing Software (SPS) software.

GEDAE was identified as the leading candidate for a number of reasons:

- overall mix of tool capabilities
- executable model concept
- repeatable testing on host and target
- target mapping toolset
- multiprocessor mapping
- ease of use
- developing signal processing functionality
- porting to different hardware platforms
- applicability to T2 SPS development
- ability to incorporate legacy C code
- in-built function libraries

Following further discussions between BAE SYSTEMS, EADS and BHDS, it was decided to take the evaluation of GEDAE further (see section 4).

## 2. Relationship with BHDS

The CAPTOR programme has a licencing agreement with BHDS which includes consultancy as well as user licencing and training. Through this, a close relationship has been established between key CAPTOR GEDAE users and the BHDS developers. This has been a major factor in the success of the CAPTOR development to date.

## 3. The CAPTOR Pilot Study

A pilot study using GEDAE to implement a real CAPTOR SPS mode and run it on a COTS target platform was identified as the

best way to ensure that GEDAE was the appropriate tool for CAPTOR SPS development.

### 3.1 Overview

A new development process was proposed for the T2 signal processing software, and a key element identified in achieving faster development times was the effectiveness of the GEDAE tool.

The study was undertaken to obtain detailed knowledge from the use of this proposed development process, to determine the efficiency of the new process, and to assess the capability of the GEDAE tool when used to develop a significant radar signal processing application.

A basic radar mode (a medium PRF mode) was selected and modelled in GEDAE for the study.

Given that the target UVP hardware was still at the design stage, a Sky Computers Rapid Development System based on two Merlin quad G4 cards, controlled via a Sparc processor, was used as the target platform.

### 3.2 Pilot Study Objectives

The study concentrated on investigating the main new areas in the development process and the key features of the GEDAE tool:

- Use of GEDAE tool to model algorithms and host test them using algorithm test vectors
- Use of GEDAE tool to model radar modes and host test them using radar mode test vectors
- Generation of target code using autocode generation features of the GEDAE tool
- Optimisation of the GEDAE host graph to run on a multi-processor target

### 3.3 Pilot Study Results

The signal processing for the selected CAPTOR Radar mode was implemented in GEDAE using the proposed T2 process. The processing was optimised and demonstrated to run sufficiently quickly when distributed across representative multiple processors. Further optimisation could be achieved if necessary, but there is clearly a trade off between optimisation of processing against the associated cost and at present this is judged not to be cost effective.

Refinements to the development process for the main T2 signal processing software have been identified as a result of carrying out this work.

As a result of the pilot study, GEDAE was selected for use on the full scale T2 SPS development, and the refined development process was adopted for use.

The performance data generated in this study has been used as the basis for the partitioning strategy for the T2 signal processing.

The metrics that were gathered were used to calculate initial baseline costs for the development of the T2 signal processing. These will be continuously refined as T2 development continues and more metric data is gathered.

### 3.4 Learning from the CAPTOR Pilot

A good example of how the relationship between CAPTOR and BHDS has been of benefit is the GEDAE evolution resulting directly from the CAPTOR pilot study. The pilot study developed a CAPTOR design concept: however this was not realisable with the version of GEDAE available at that time (Version 3.1 and 3.2 were used during the pilot).

The radar mode implemented in the study, in common with many of the CAPTOR signal processing radar modes, applies the same processing to a number of different sized input data sets; this may vary with PRF for example. This was implemented for this study by using variable matrix representations in GEDAE. This allows one GEDAE graph to handle all of the possible data sizes. However this forces GEDAE to use dynamic scheduling, which is less efficient than static scheduling and leads to performance loss. To implement the same graphs with fixed matrix representations (and hence static schedules) would at the time have led to a large increase in complexity of the graphs and was not a viable option.

A GEDAE modelling concept based on the simplicity of a fixed size matrix implementation but with limited flexibility to handle different data sizes was identified to be the best solution.

The CAPTOR team worked closely with BHDS to identify the real requirements, and as a result, the static enumeration features were added to GEDAE Version 4 to support CAPTOR. This allows the performance benefits of static schedules to be exploited for situations where a dynamic data structure is required and can be relatively easily enumerated without significantly increasing the complexity of the GEDAE graphs.

## 4. Entering Full Scale CAPTOR Development

Full-scale development started in late 2001, with an initial period of time spent setting up the teams and the development environment.

### 4.1 Managing GEDAE Changes on CAPTOR

The GEDAE tool has evolved during the time-span of the CAPTOR T2 program, and the project modelling activities have been tailored to use the latest version where possible.

Full-scale development began using V3.4, but the design was targeted to operate fully only once additional features became available (enumeration, exclusivity). The design is also upgradeable to use additional features such as state variables.

The new features in GEDAE Version 4 are being exploited to improve the CAPTOR models.

### 4.2 Setting Up a Software Development Environment

CAPTOR T2 development is taking place in a predominantly PC/NT environment. These PC platforms are being used for all Host Model generation, integration and testing.

A Solaris based platform is being used to allow the Host models to be ported to representative target platforms for testing and optimisation only.

The GEDAE tool provides many of the capabilities required for the software design lifecycle; however it still needs the support of

a requirements management/ traceability tool and a code management/ configuration management tool for use on a major defence programme such as CAPTOR.

The need for an interface between GEDAE and these two tools was identified and discussed with BHDS, who have now included suitable capabilities into GEDAE.

The Requirements Management tool interface allows hyperlinks to be added to GEDAE workproducts. Scripts can be embedded in these links to launch the tool and also to mark the files for traceability purposes.

For the CAPTOR programme, the requirements are in text form, and the GEDAE workproducts will be included in the tool as the design layer, with links from the GEDAE workproducts to the appropriate requirements.

The CM tool interface within GEDAE allows GEDAE to be interfaced to any CM tool and tool specific commands can be embedded behind generic GEDAE commands (e.g. check in, check out, difference etc).

### 4.3 Process Definition

The development process adopted for the SPS is based on an iterative incremental software lifecycle which allows the on-going refinement of the process throughout the duration of the project. [1]

An initial study identified the candidate algorithms which can then be used to assemble all of the radar modes in the SPS.

The T2 SIP software development process comprises the following activities:

- Generation of a clear, concise description of each algorithm by extracting an implementation independent description of the algorithm from the T1 SIP software documentation. The set of T2 algorithm descriptions form the Algorithm Description Document or ADD.
- Construction of a GEDAE model of the algorithm
- Building of a test harness in GEDAE for the algorithm and construction of simple test vectors to test the basic functionality
- Testing of each algorithm on a host and then on a representative target
- Peer review of each algorithm followed by a structured inspection – a technique designed to investigate and question the behaviour of the workproduct in a team environment
- Building of sub-modes, formed by grouping algorithms together – these are also tested and subject to structured inspection
- Evaluation of these higher level work products more fully on the target where benchmarking is carried out to identify areas where rework may yield improved performance, and also to define the initial target hardware partitioning
- Assembly of modes and further test and inspection.
- Partitioning of modes across the target hardware and optimisation until they meet timing requirements.

- Re-testing and re-inspection, if necessary, depending on the changes made at this stage

An overall framework for the signal processing software is built up using the same process. Complete modes are then integrated into the framework to build up the complete SPS application.

A documentation set has been created, which define the T2 SPS development process to comply with the companies’ standards for software development documentation.

The documentation set comprises:

- A Software Development Plan defining the basic process to be followed and tools to be used at a high level.
- A Software Standards and Procedures Manual (SSPM) defining the process steps in detail.
- A Code of Practice for SPS development defining in detail how to use the tools (GEDAE in particular) to carry out the process defined in the SSPM. It also includes a project ‘coding standard’ for GEDAE modelling which defines project rules for flowgraph layout, headers, comments, naming conventions etc.

### 4.4 Setting up the Development Team

At BAE SYSTEMS, a mixed team of about 20 software and systems engineers has been established – all have been trained in GEDAE, and several have been through the advanced training from BHDS. A similar team has been established at EADS and similar training and preparation undertaken.

### 4.5 Software Architecture Definition

The SPS GEDAE model is made up of a basic framework which handles data IO and a controller which controls data routing, into which each of the radar modes can be integrated. [2] This is shown in Figure 2.

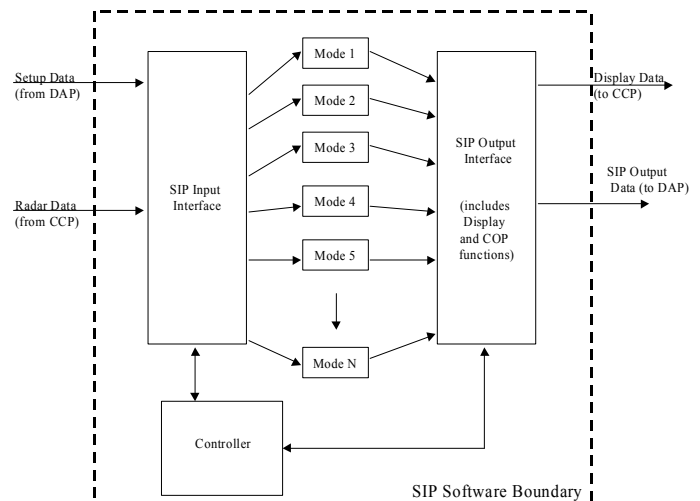
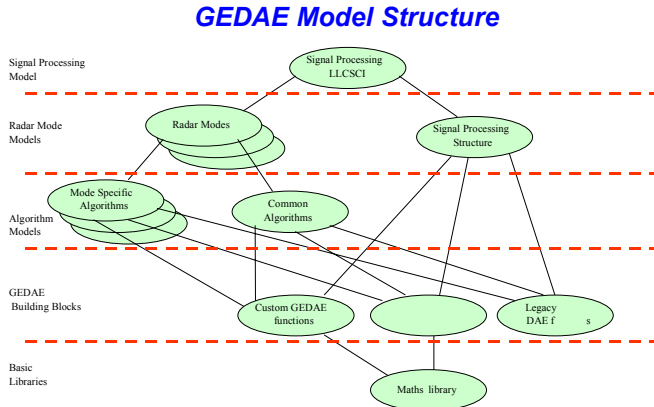


Figure 2 – The CAPTOR SPS Model Functional Structure

The radar modes themselves are made up of algorithms which each capture a single signal processing function – thus maximising reuse potential.

Each algorithm can be a primitive, a GEDAE flowgraph, or can be encapsulated legacy code from T1.

A basic model logical structure has been identified as shown in Figure 3.



**Figure 3 – The CAPTOR SPS Model Logical Structure**

The radar modes to be implemented in T2 are already defined and specified in the T1 baseline. These T1 mode specifications have been decomposed into algorithms, and common algorithms have been identified to exploit the potential for re-use within the processing. An estimate at T1 is that there are approximately 2000 algorithms in the signal processing modes, and initial analysis indicates that this can be represented by approximately 250 common and 400 mode specific algorithms of similar size and complexity.

The philosophy adopted for generating the GEDAE models of the algorithms is to use GEDAE standard library components as much as possible, rather than generating custom components. The exception to this rule is for legacy software, where the philosophy adopted is to repackage the existing T1 C code and create GEDAE wrapper boxes, to allow the code to be linked to the remaining GEDAE model.

### 4.6 Joint Working

The radar modes are split between EADS and BAE SYSTEMS. Initial work was carried out to identify where common algorithms would be needed by both EADS and BAE SYSTEMS, and development of these was also shared.

To develop a radar mode, a small team (typically 1 Systems and 1 Software engineer) work together. They initially identify the algorithms which make up the mode, and check which of these are already constructed and can be reused. Any new algorithms are modelled in GEDAE and tested standalone on the host and representative target. All algorithms are added to the common pool of algorithms for future reuse. Once sufficient algorithms exist, sub-mode models are constructed and further tested; this build up of functionality continues until the whole radar mode is integrated and tested as a mode.

Once modes are complete, they are integrated into the overall SPS framework by BAE SYSTEMS.

### 4.7 Hardware Mapping

A round robin processing scheme has been chosen for the SPS. In the past, bandwidth limitations have meant that signal processing solutions such as T1 have been configured in pipelines.

The advantages of a round robin scheme are that it is flexible and easily expandable, and also allows the overall latency to be controlled.

Outside of the round robin pool of processors a single G4 processor is allocated as the overall controller and a further single G4 processor is allocated to carry out necessary legacy processing downstream from the round robin.

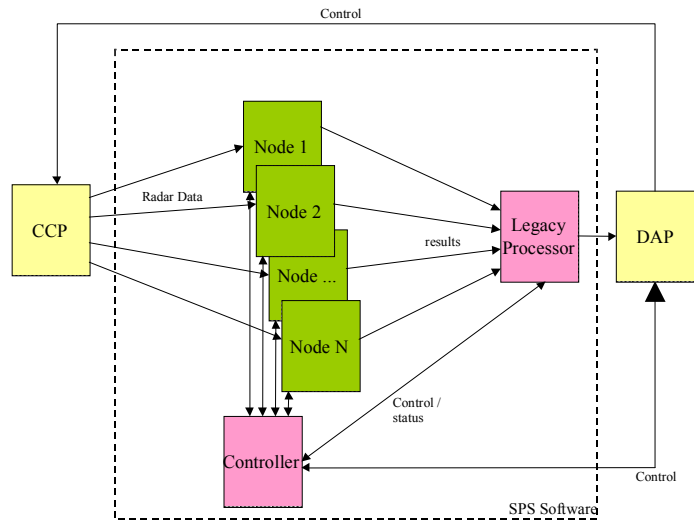
The remaining G4 processors are divided into equal groups (nodes). The number of processors in each node can be modified, but for CAPTOR, the following rules have been adopted:

- All of the processors in a node are on the same UVP
- The number of nodes is limited

Each node has

- an SPS Input Interface to receive data
- an interface to the controller to receive routing and control information and to return status information
- an SPS Output Interface
- a copy of the software for every mode

This is shown in Figure 4.



**Figure 4 – Round Robin Concept**

The mode models on each node are then distributed across the processors within the node to meet the processing timing requirements for that mode.

All of the round robin set up variables (e.g. number of processors per node, number of nodes) are parameters in the GEDAE model, so the round robin can be quickly tailored to suit different hardware architectures or to handle software requirements changes.

For example 4 nodes of 3 processors could quickly be reconfigured to 3 nodes of 4 processors if the latency requirements were increased.

The initial design concept was to have a separate round robin controller, designed and built using a UML based OOA/ OOD tool. However following discussions with BHDS, it was decided to include this in the GEDAE SPS model. BHDS worked with the CAPTOR team to develop a generic prototype framework, which can be tailored for CAPTOR use. The specific CAPTOR requirements have been identified and addressed as part of this process, and where necessary, BHDS have included features to support these requirements.

#### **4.8 Current Status of CAPTOR**

Good progress has been made so far on CAPTOR.

Initial iterations of the lifecycle concentrated on identifying, specifying and generating a library of common algorithm GEDAE models. These are now in place and have been reviewed.

Initial modes to be developed were selected and the additional algorithms for these modes have also been generated in GEDAE.

Those parts of the SPS where suitable legacy C code is available at T1 have been identified, and the legacy code has been encapsulated in GEDAE wrappers and tested against the T1 system.

Initial modes have been modelled in GEDAE and these have been reviewed. Some testing of these has been carried out by feeding identical data through the T1 Signal Processing and comparing the results. These tests have identified some minor bugs that have been resolved.

The initial modes have been ported to the Sky Development System and run on a single G4. Benchmark timings have been taken and these indicate that the modes run within their required timings.

The SPS framework has been developed from the initial prototype, and has been tailored to have the correct external data interfaces, and to have suitable interfaces for the modes and the legacy code. This has been tested using GSIM to demonstrate the multi-processor capabilities.

The initial set of modes have been integrated into the framework and tested, and further modes are being added as they become available.

#### **5. The Way Ahead**

The process of developing algorithms and modes will continue over the next 12 months. Work will also be started to partition the processing of each mode between the processors in each round robin node. It is hoped that the amount of model rework at this stage is minimal, since the host models have been benchmarked on the representative target hardware and demonstrated to run close to the specification on a single processor. In a few areas, some additional functionality may be needed in the target model to split and then recombine data for the purposes of distributing processing, but if possible this will be avoided.

One of the key areas still to be solved for the SPS is how to start up and run the GEDAE model in the deployed hardware. BHDS have been developing new features for GEDAE and over the next few months, these will be evaluated to identify the best solution for CAPTOR.

Further work will also be needed when the target platform becomes available, to develop and integrate the real time data interfaces for data input and output.

#### **6. Acknowledgements**

The authors acknowledge the support of the various colleagues at SSD Crewe Toll who contributed to this work.

#### **7. REFERENCES**

- [1] Thomson, C The CAPTOR GEDAE Development Process GUC2003
- [2] Swanson, D Mode Control with GEDAE D. Swanson GUC2003